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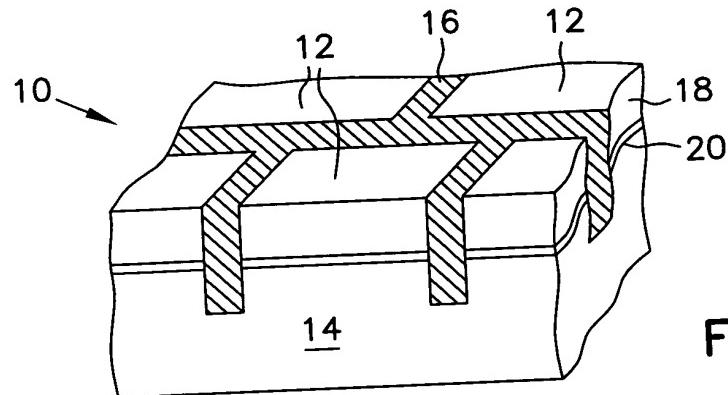


FIG. 1A

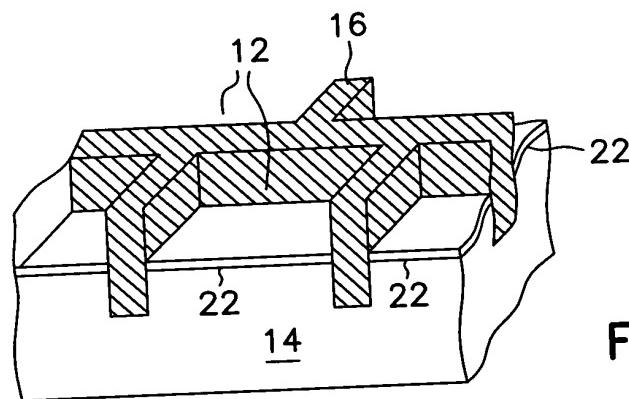


FIG. 1B

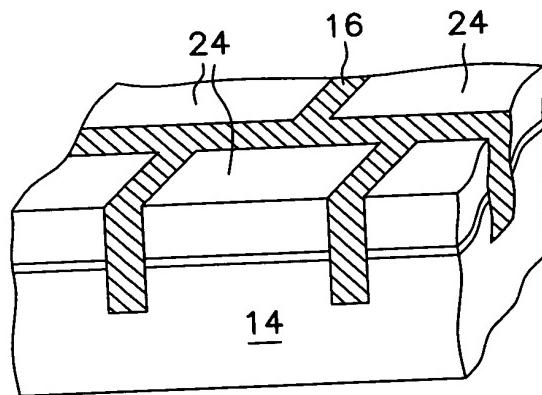


FIG. 1C

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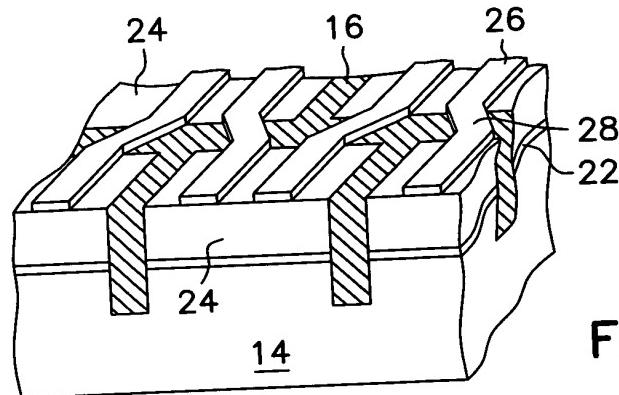


FIG. 1D

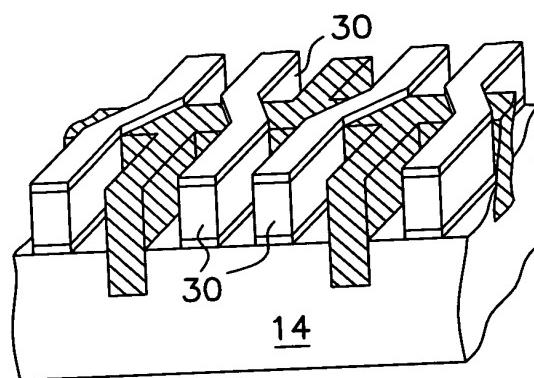


FIG. 1E

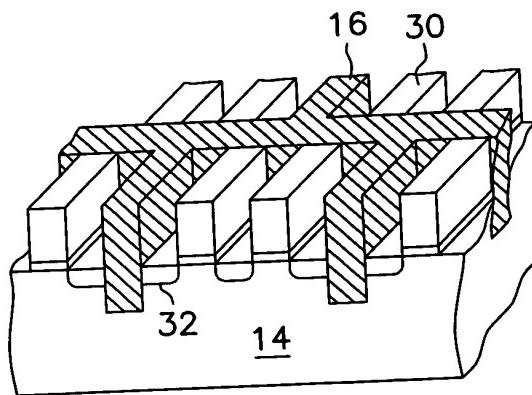


FIG. 1F

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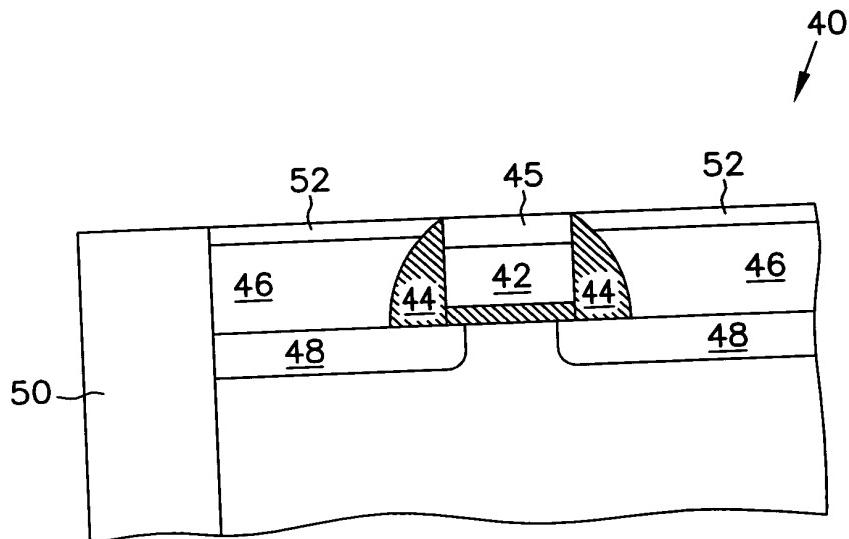


FIG. 2A

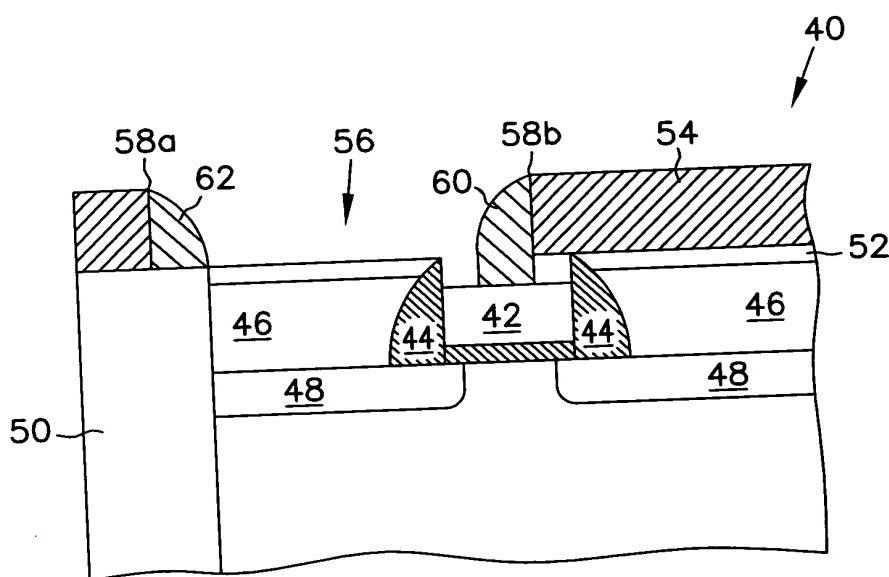


FIG. 2B

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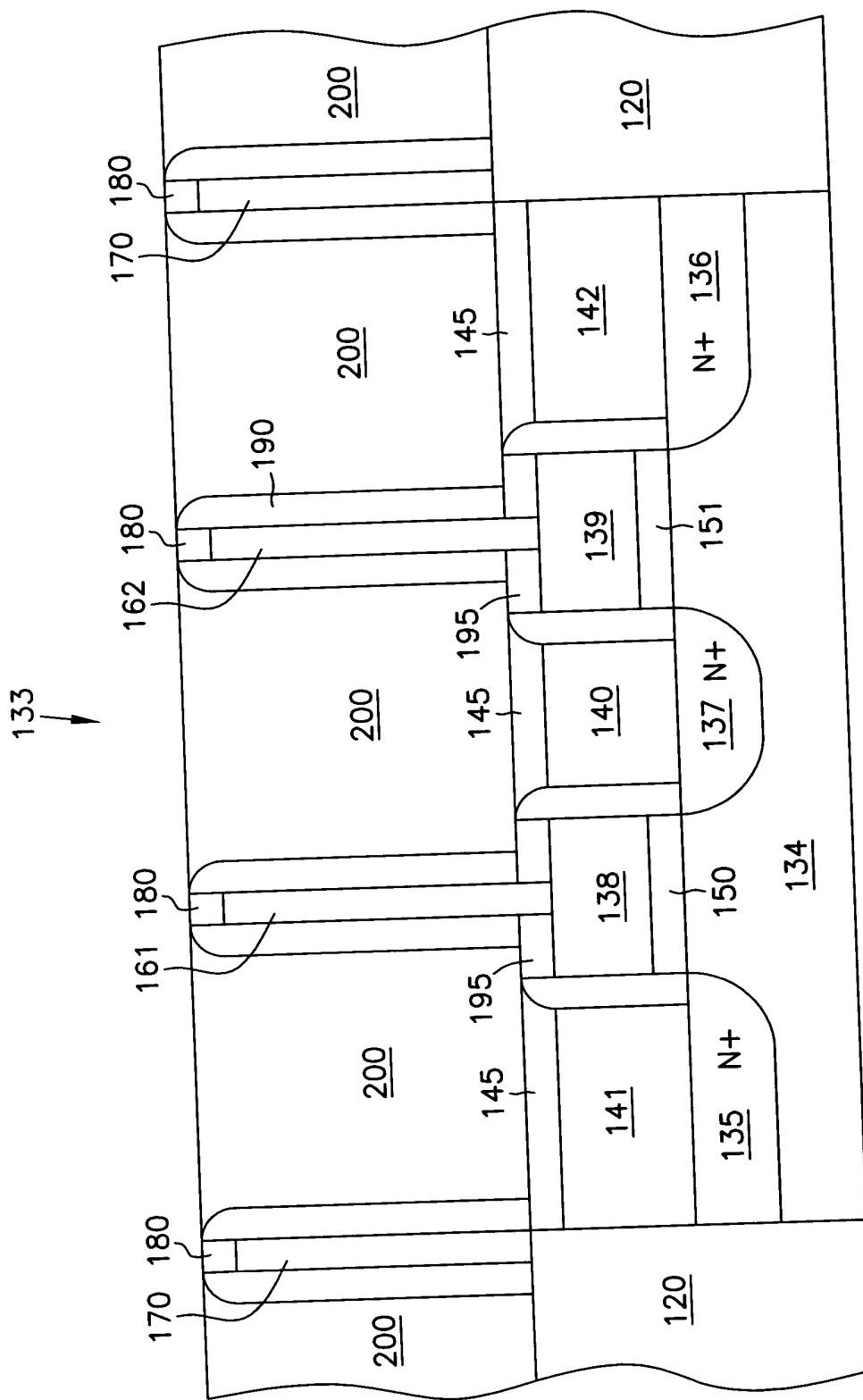


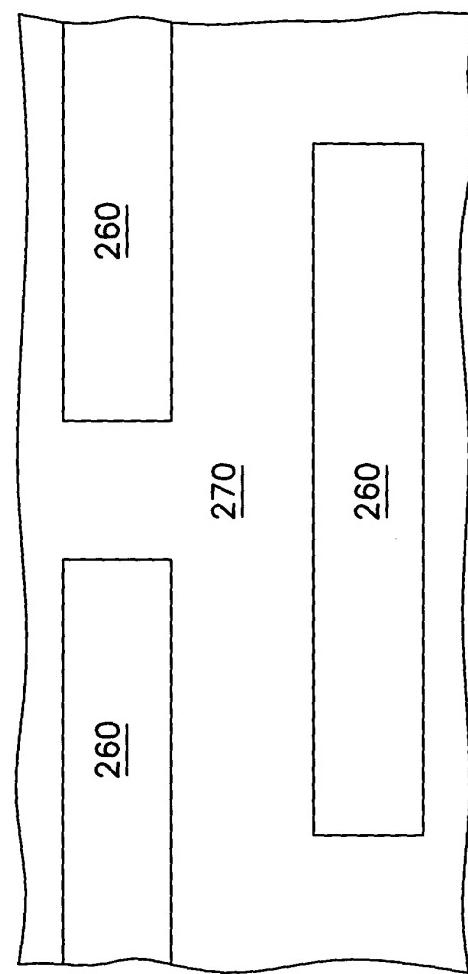
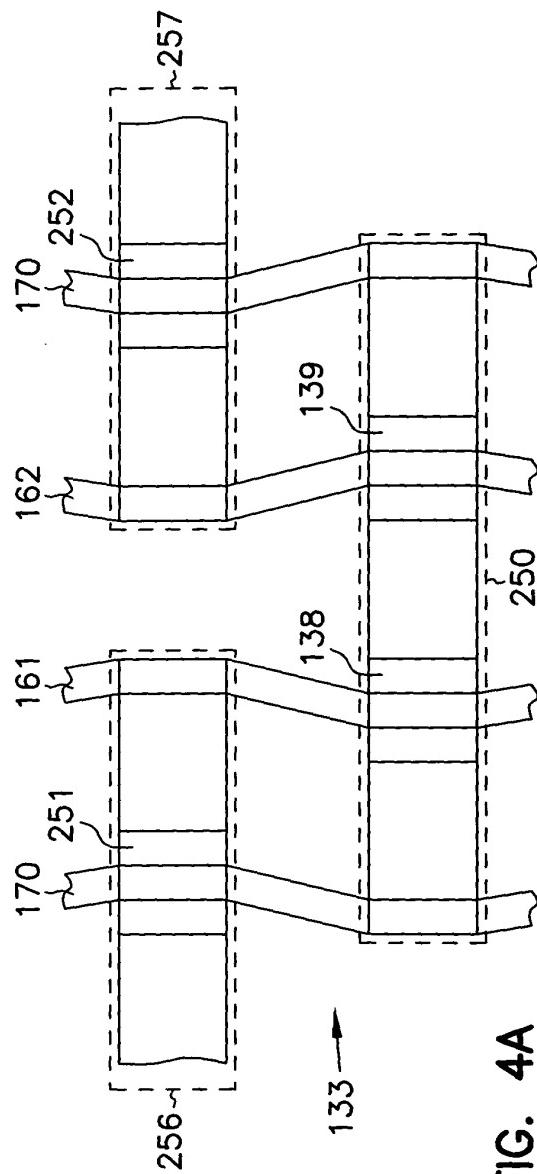
FIG. 3

TITLE: METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED CIRCUIT

INVENTORS NAME: Wendell P. Noble Jr.

Dkt #: 303.257US4

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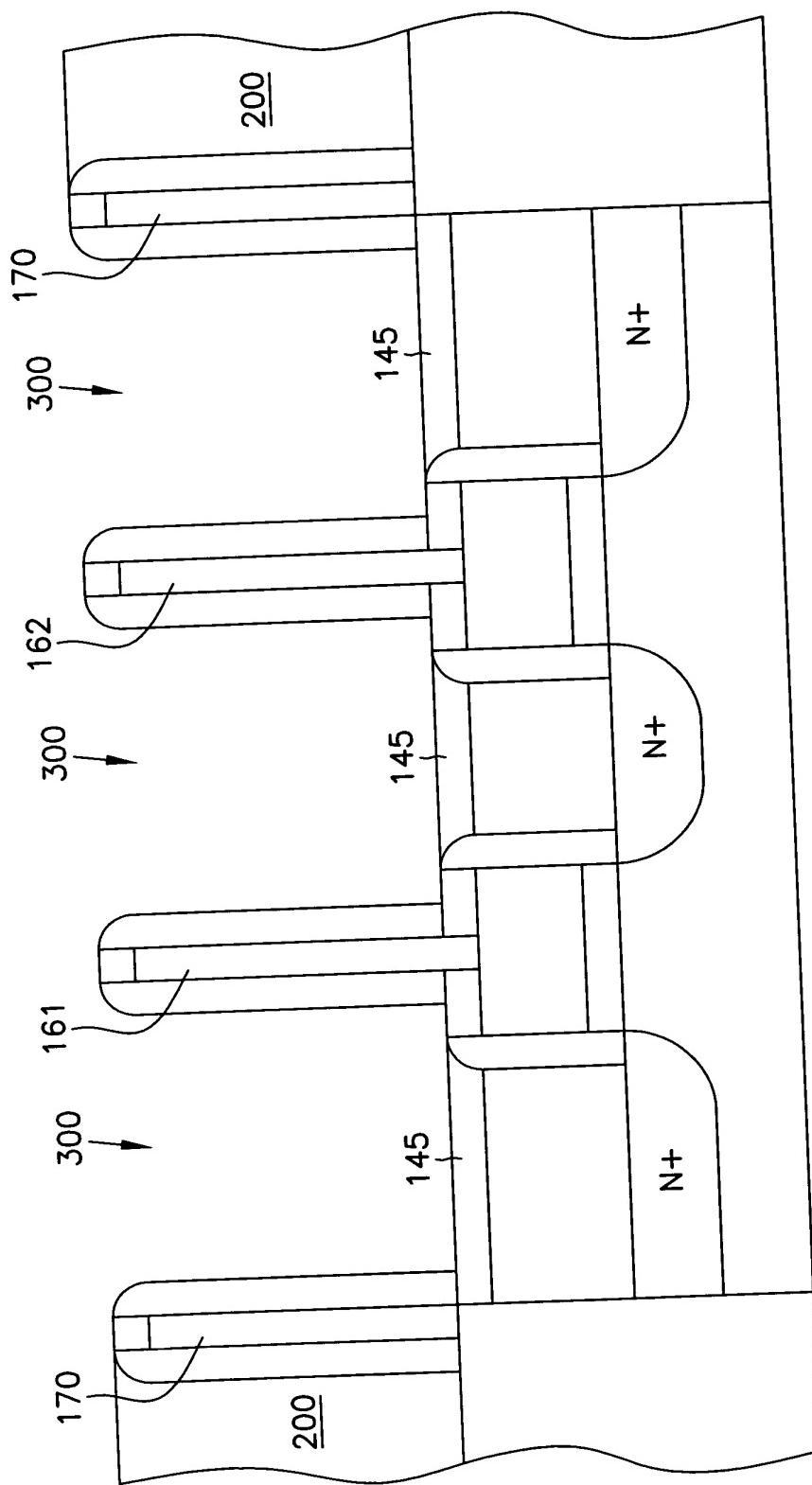


FIG. 5

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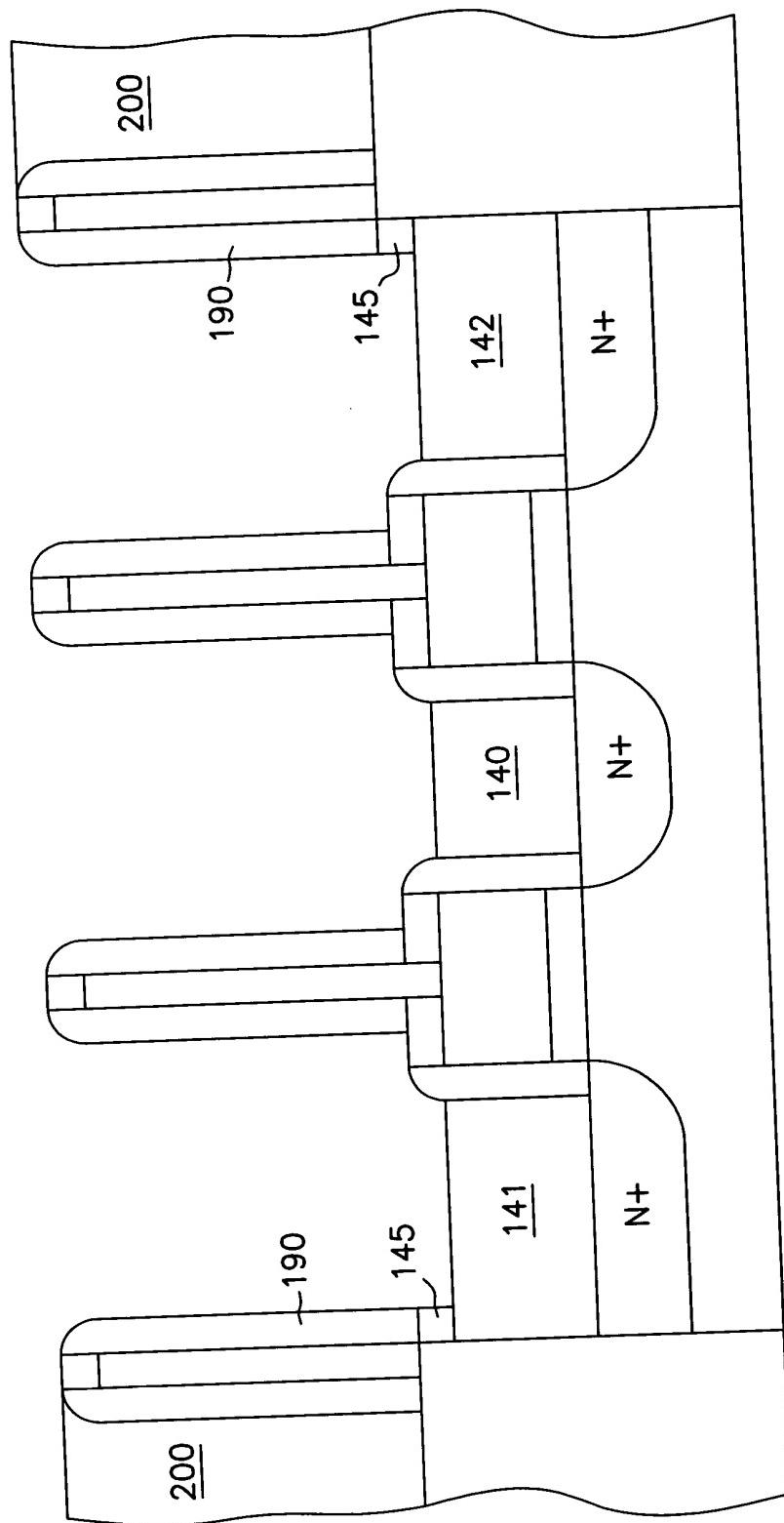


FIG. 6A

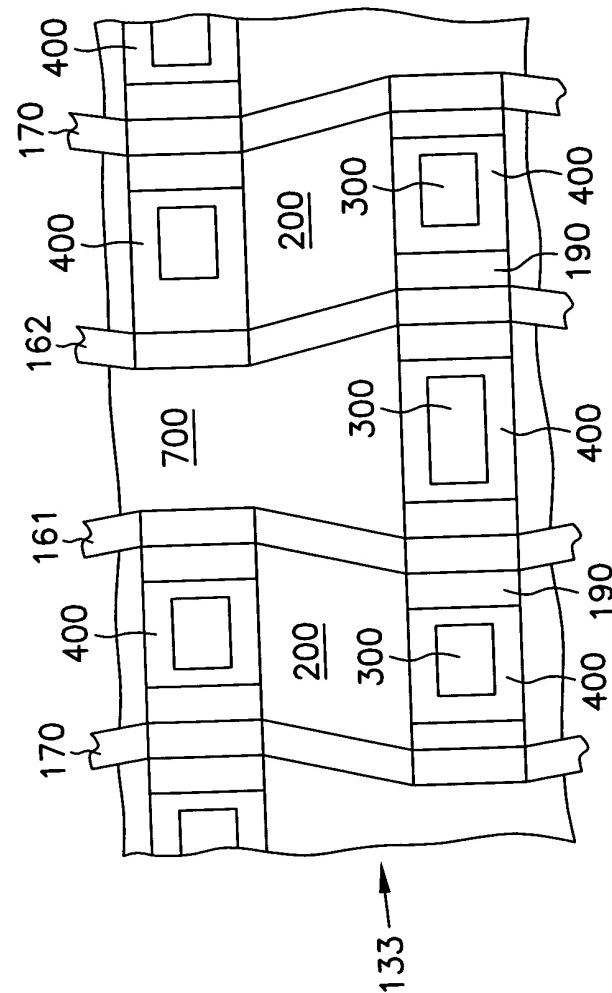


FIG. 6B

TITLE: METHOD FOR FORMING GATE SEGMENTS FOR AN INTEGRATED CIRCUIT
INVENTOR'S NAME: Wendell P. Noble Jr.
Dkt #: 303.257US4

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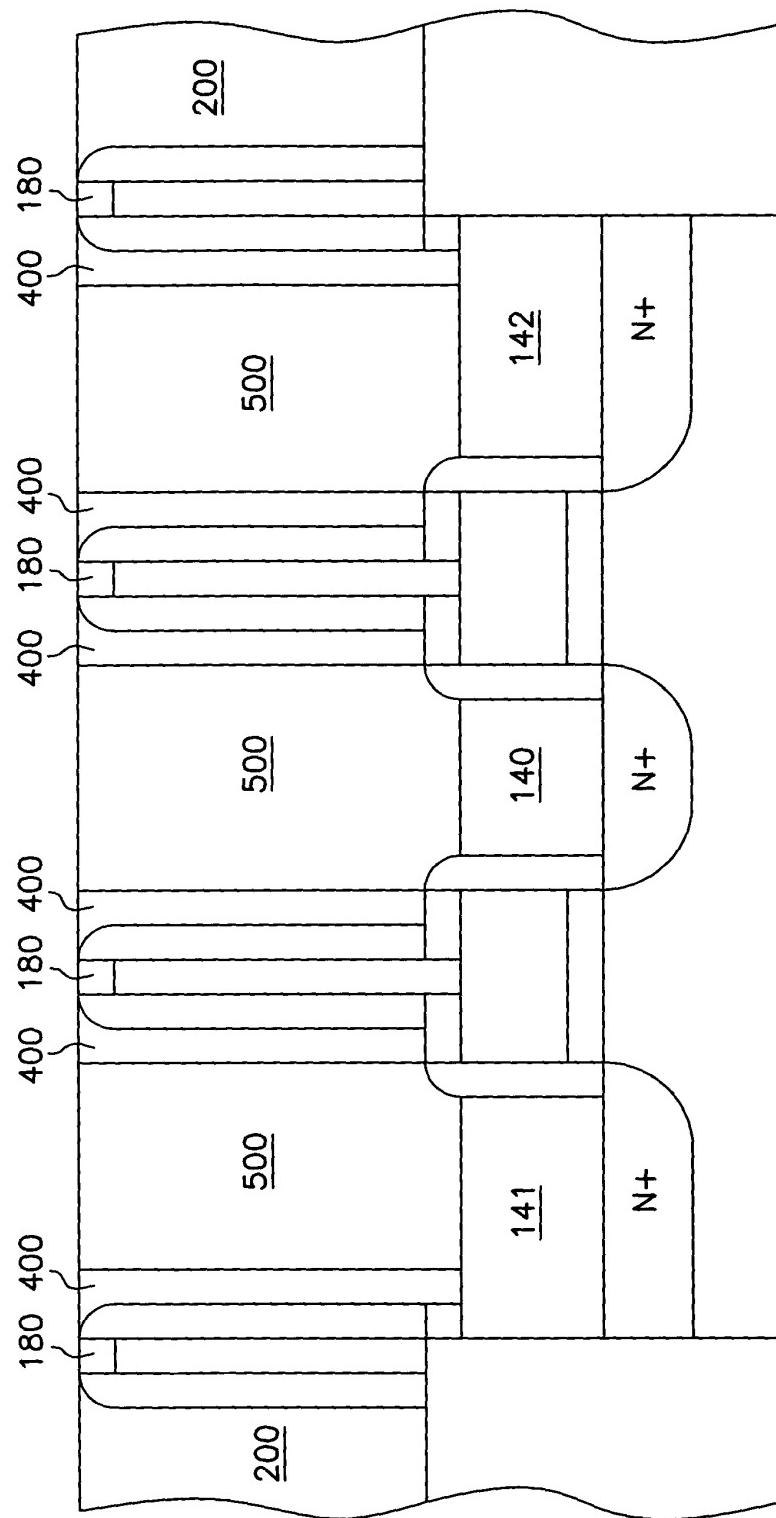


FIG. 7A

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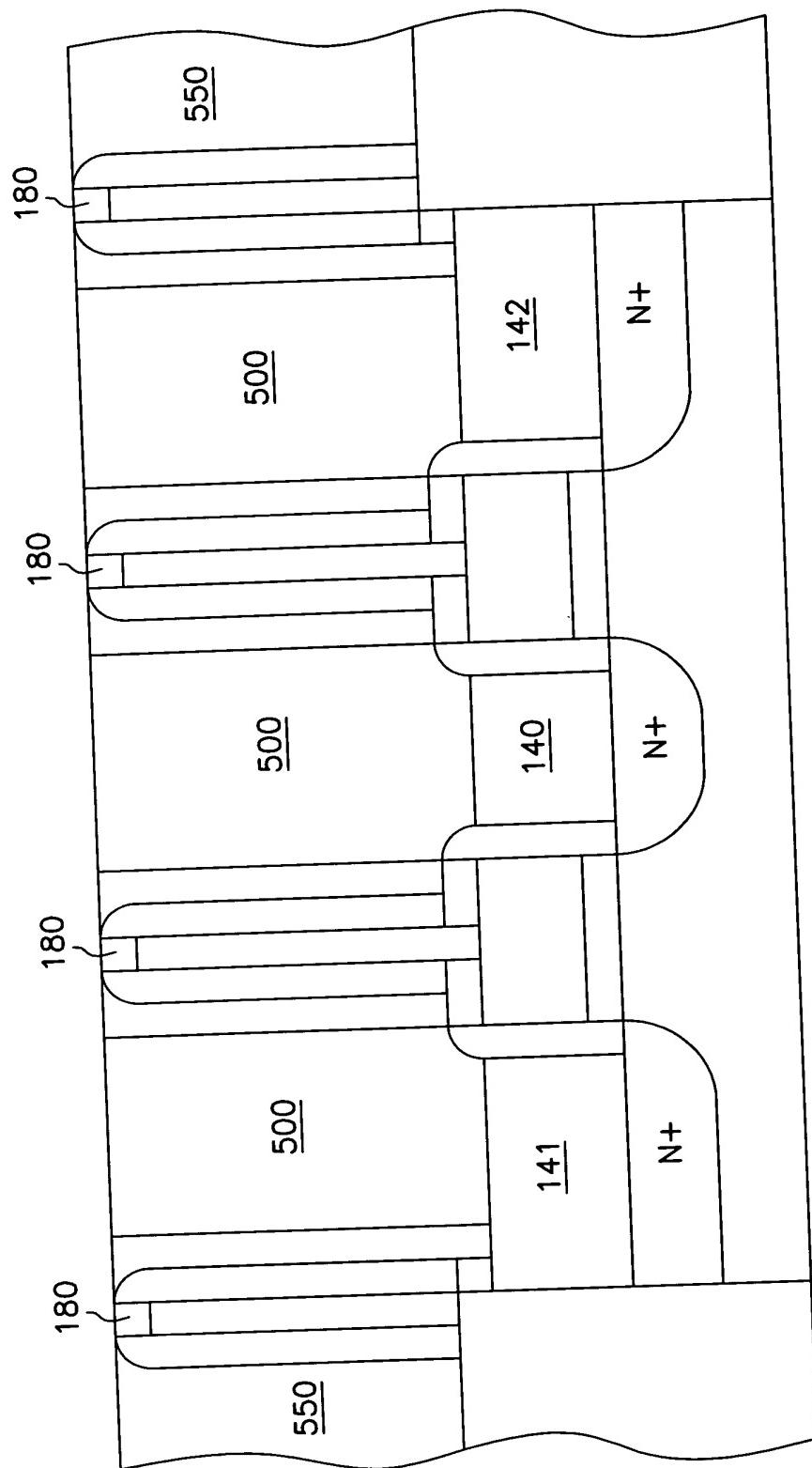


FIG. 7B

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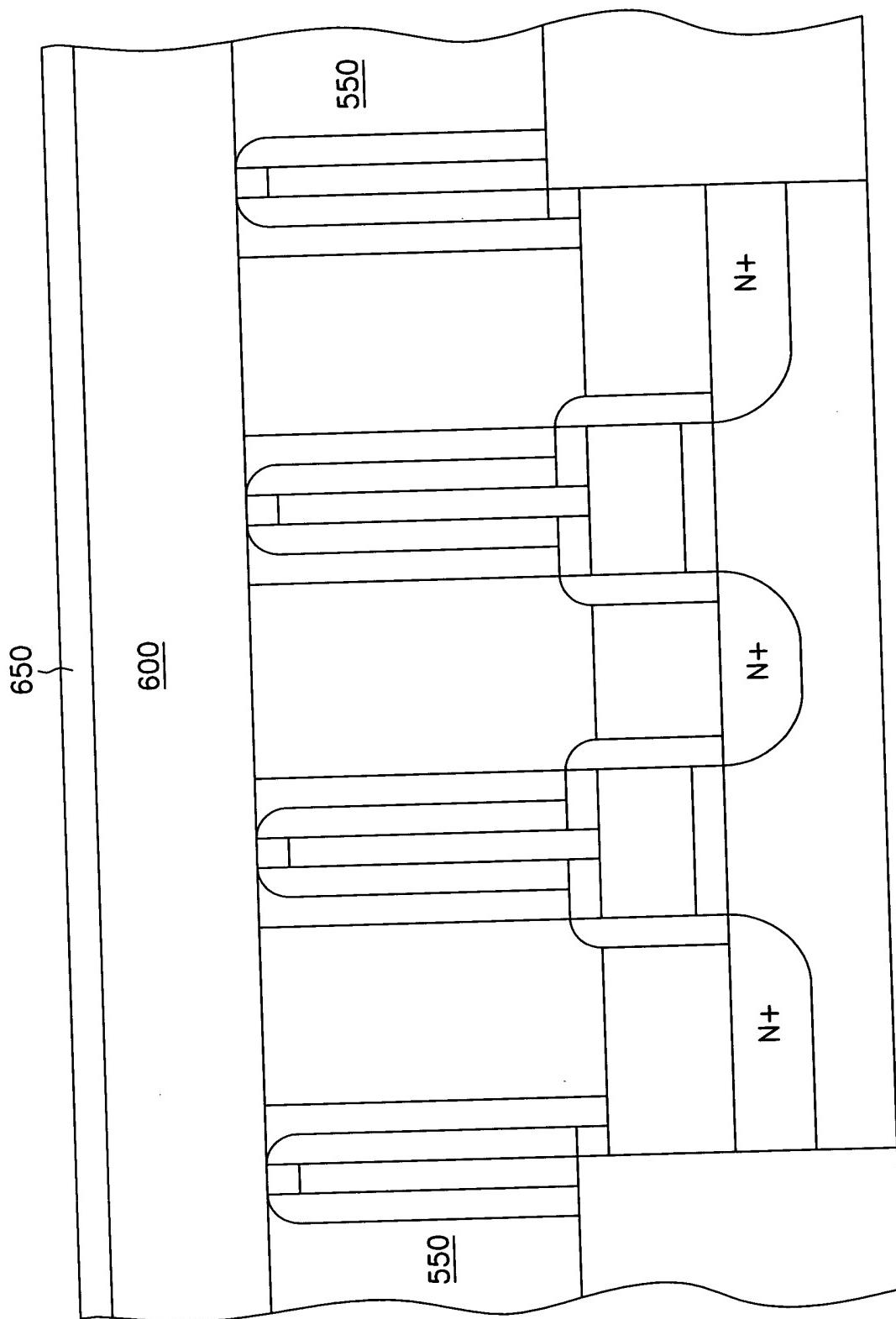


FIG. 8

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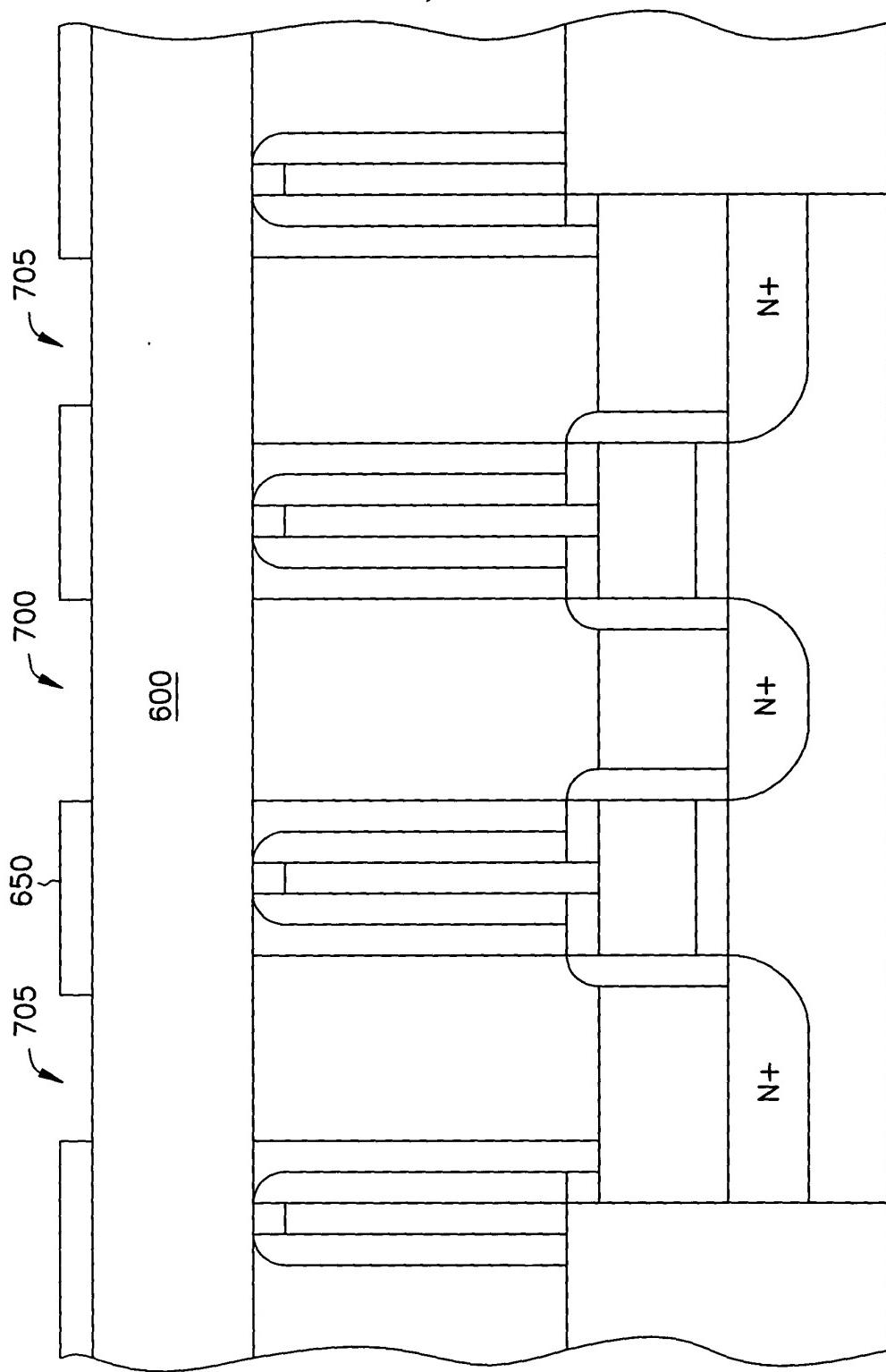


FIG. 9

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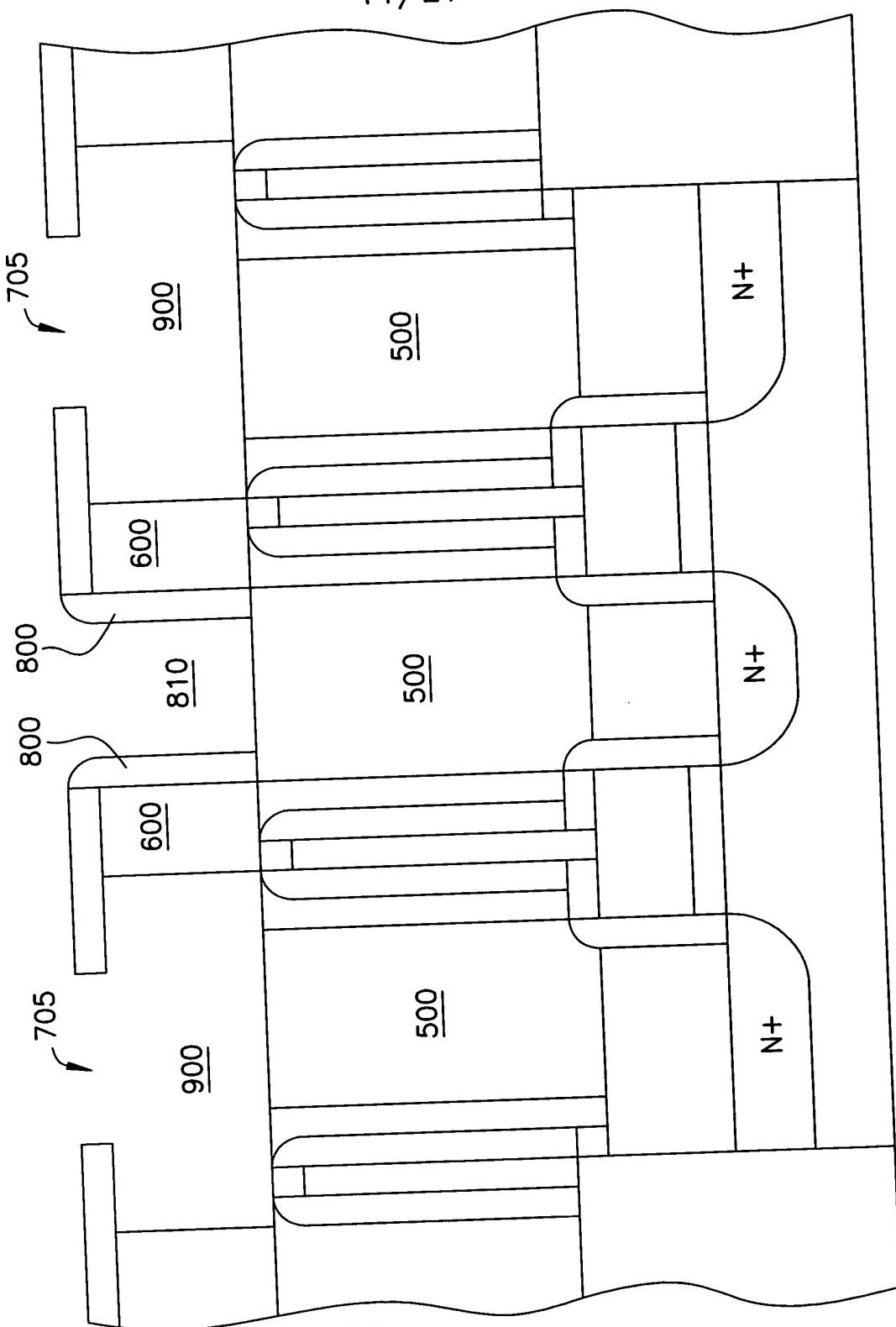


FIG. 11

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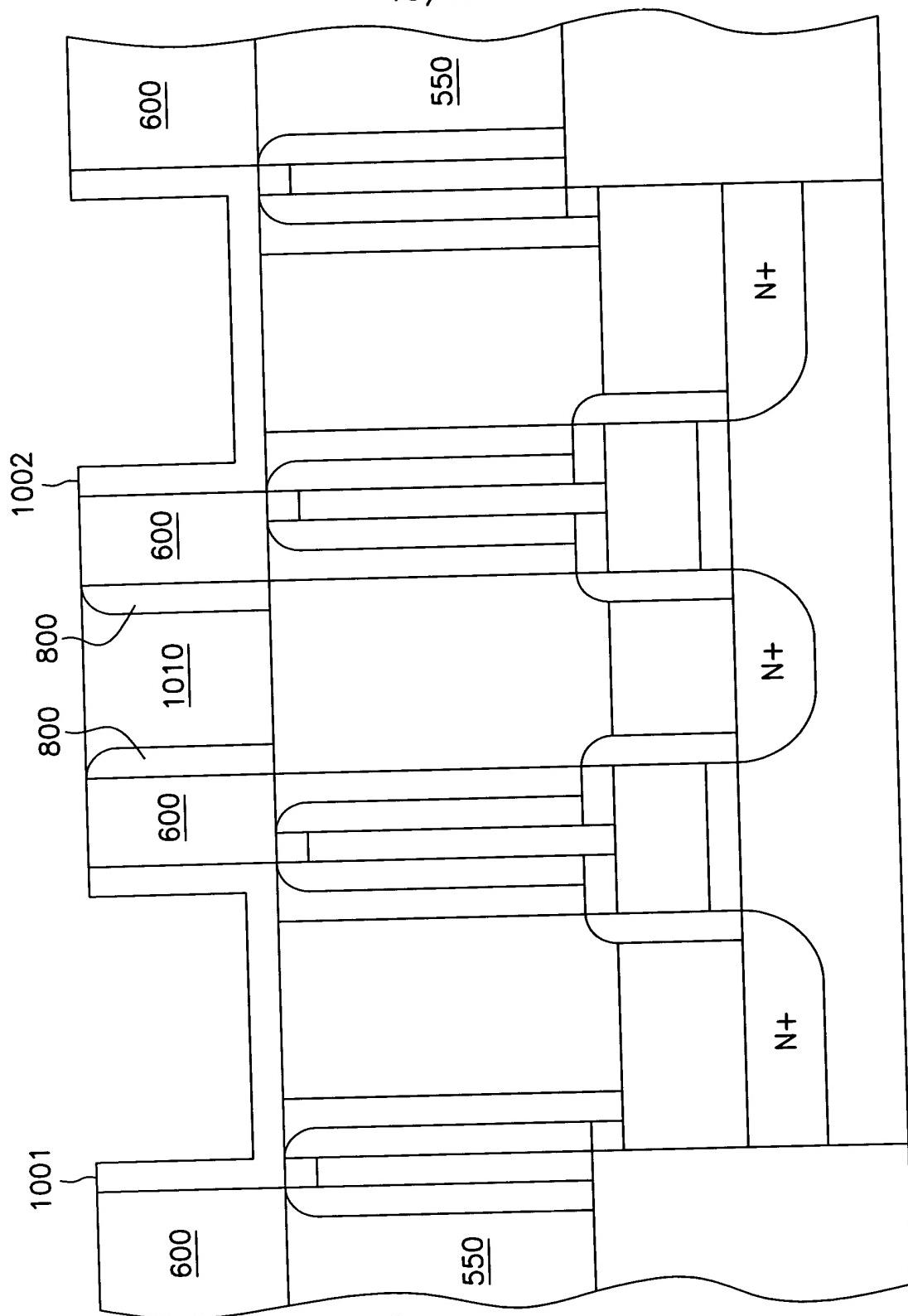


FIG. 12

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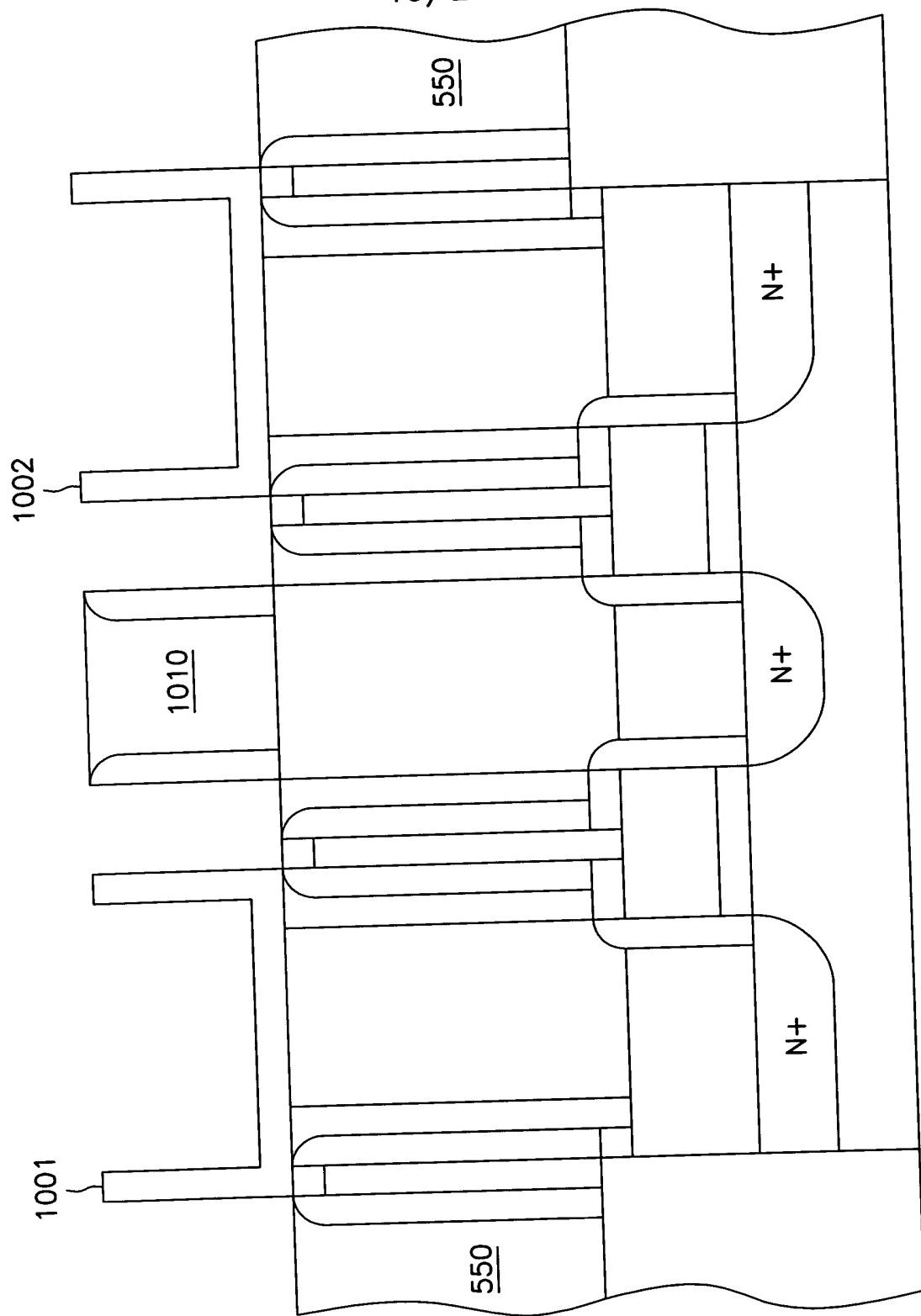


FIG. 13

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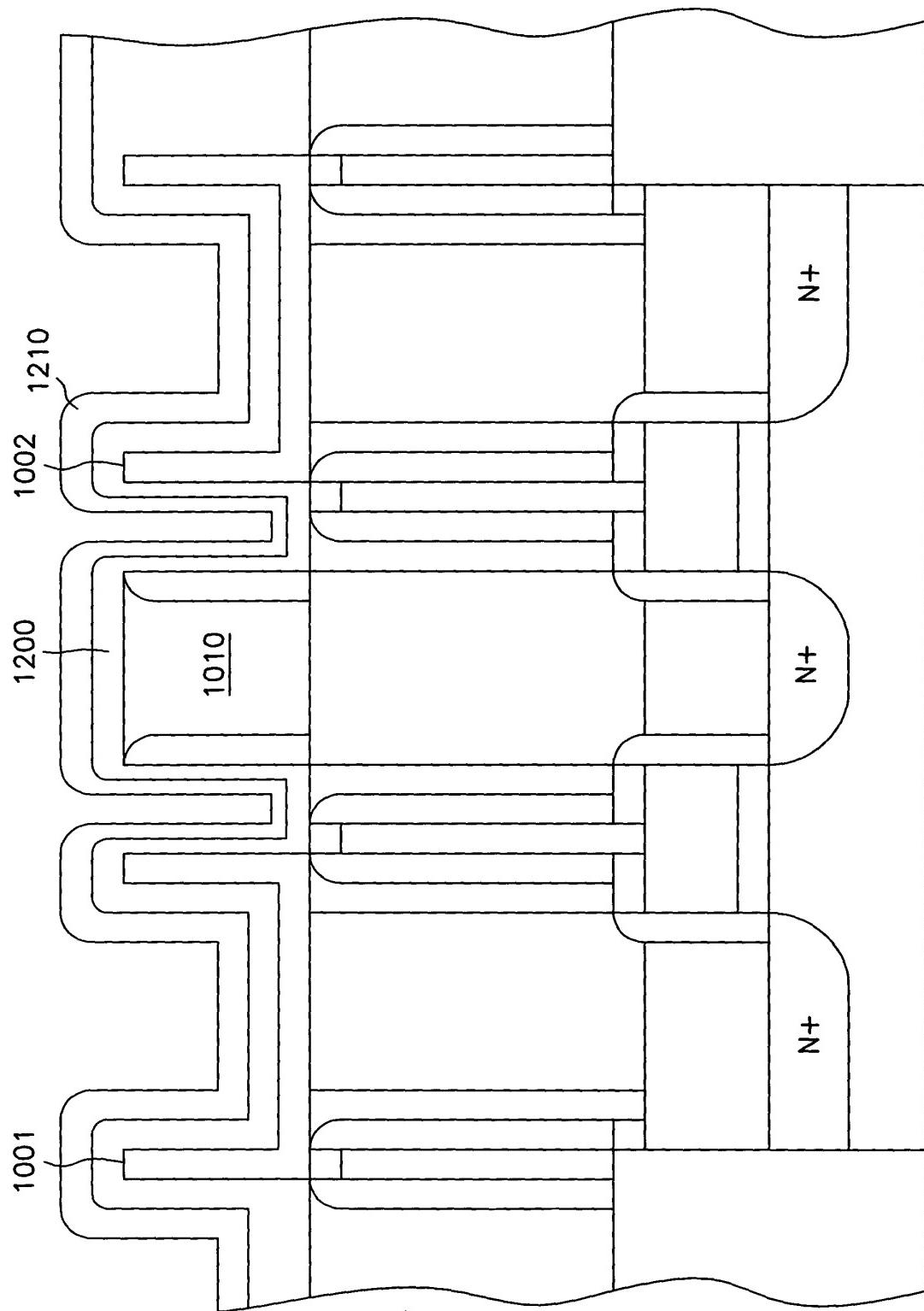


FIG. 14

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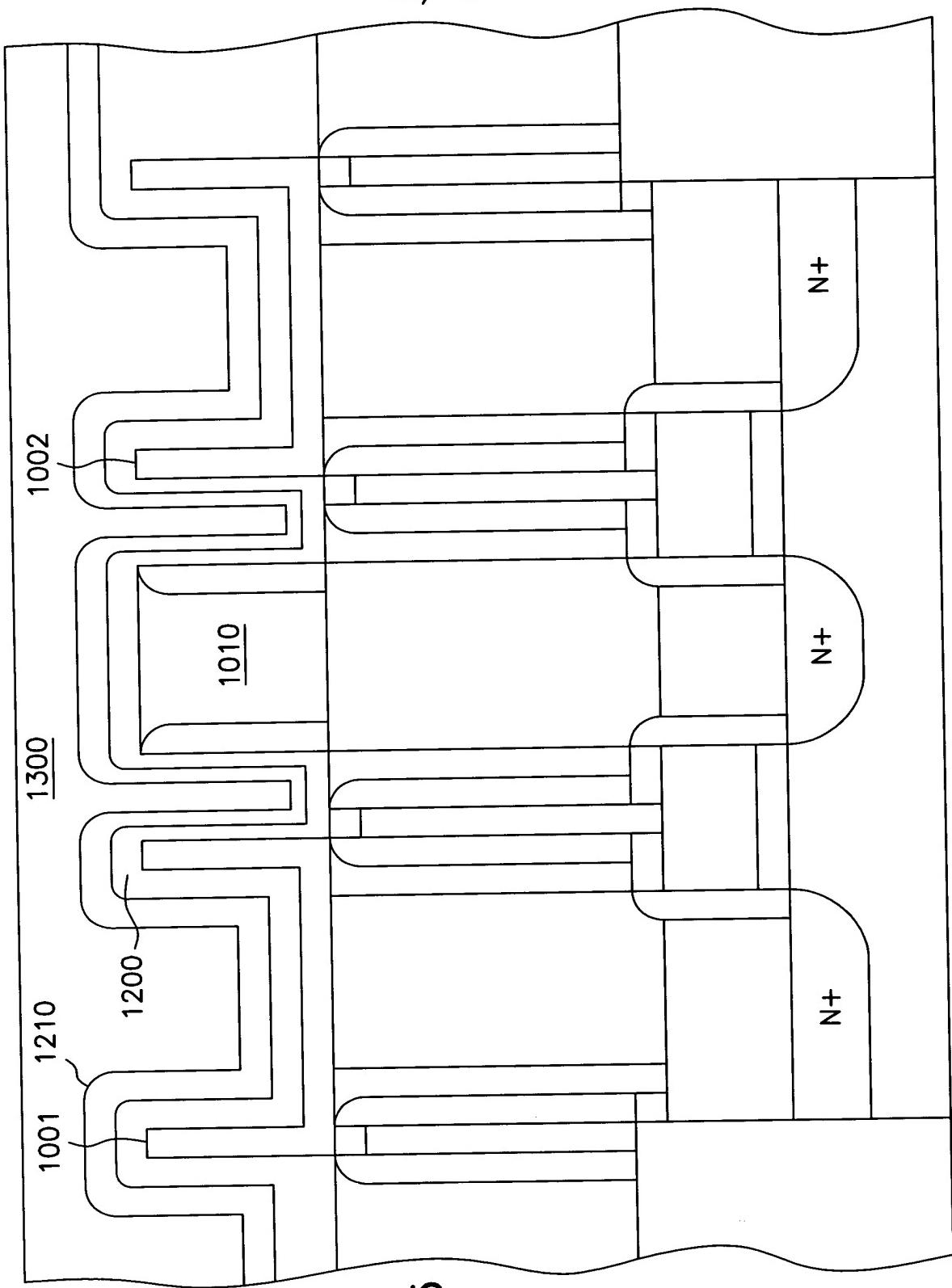


FIG. 15

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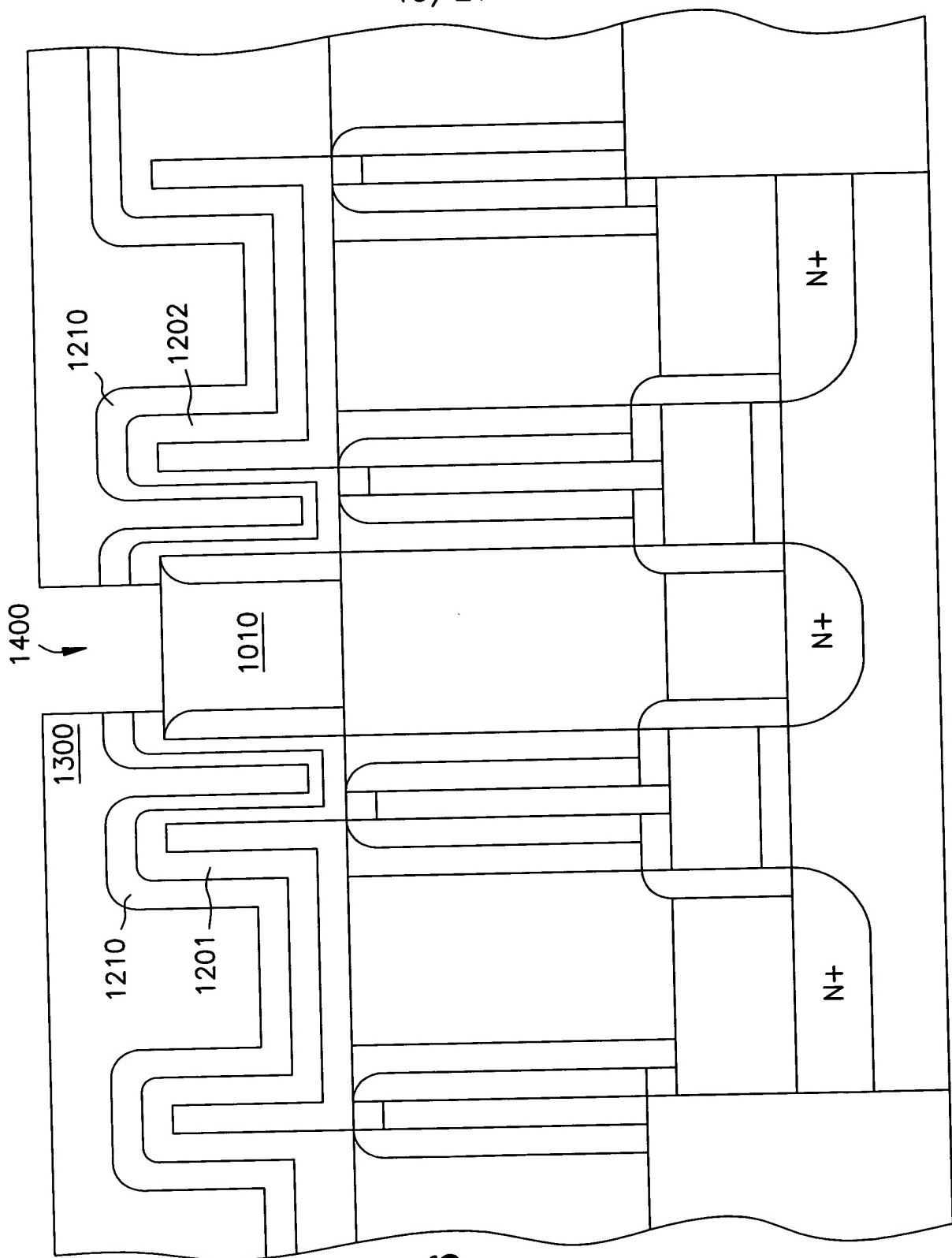


FIG. 16

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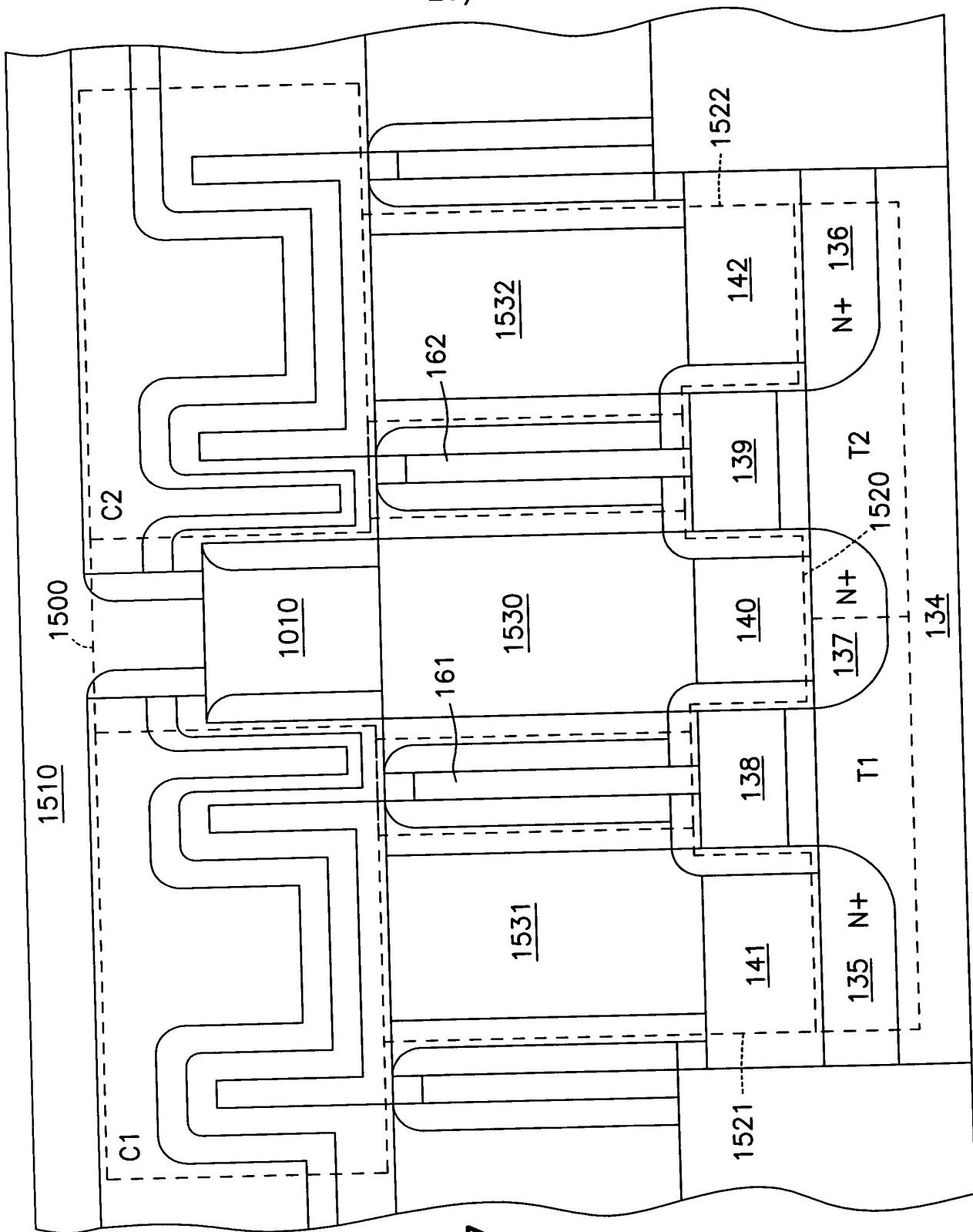


FIG. 17

FIG. 18

